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Ultrathin organic transistors on oxide surfaces

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Abstract. We have built a model organic field-effect transistor that is basically composed of a single layer of pentacene crystal in interaction with an oxide surface. Drain and source contacts are ohmic so that the pentacene layer can carry a current density as high as 3000 A cm^{-2} at a gate voltage of –60 V. Four-probe and two-probe transport measurements as a function of temperature and fields are presented in relation with structural near-field observations. The experimental results suggest a simple two-dimensional model where the equilibrium between free and trapped carriers at the oxide interface determines the OFET characteristics and performance.

In recent years, thin-film organic field-effect transistors (OFETs) have begun to be considered as a possible alternative to the hydrogenated amorphous silicon thin-film transistors (a-Si:H TFTs) used in active matrix flat panel displays and other large-area electronics applications [1, 2]. Low-temperature processability, low-cost fabrication and compatibility with arbitrary substrates are some of the promising advantages of OFETs, among others [3]–[5]. Of the many organic materials available, pentacene, in particular, is one of the leading candidates for use in current thin-film OFET architectures; this is because of its excellent electrical characteristics and its resistance to atmospheric oxygen [6]. In the recent literature, pentacene's transport properties, as well as transistor performance, have already been analysed from the point of view of substrate treatments [7, 8], pentacene evaporation rate and substrate temperature [9, 10], electrode chemical nature and channel geometry [11, 12]. To summarize, the results show that the morphology, crystal structure and molecular ordering of the first organic monolayer(s) at

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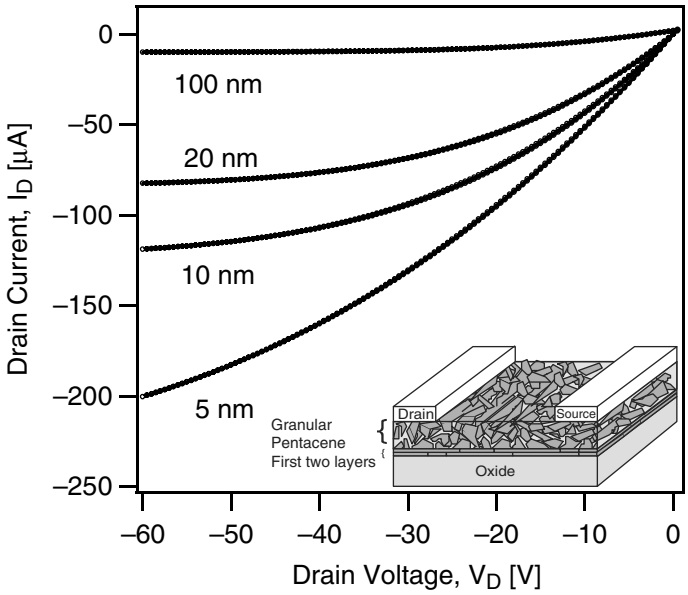

Figure 1. Current–voltage characteristics of various pentacene thin film OFETs deposited on oxide surfaces at a gate voltage of −60 V. The channel length L and width W are 100 and 6000 μm, respectively. Surprisingly, the drain current density decreases as the pentacene thickness increases. The structure of the pentacene film can be depicted as one or two perfectly grown crystalline layers on the gate-oxide dielectric followed by a granular bulk, on top of which a Au drain and source electrode are evaporated.

the pentacene/dielectric interface are essential determinants of carrier transport phenomena [9], [13]–[16].

To further investigate these interface effects, we have attempted to construct a model device which consists essentially of a single layer of pentacene on an oxide substrate. To do this, a series of thin-film OFETs with different pentacene thicknesses were fabricated on a SiO_2 gate dielectric followed by low-temperature gold deposition of the source-and-drain contacts. The pentacene film thicknesses in these devices ranged from 5 nm (ultrathin) to 100 nm. Also, before each pentacene deposition, the SiO_2 surface was activated by exposure to oxygen-plasma for 5 min in a 0.1 mbar O_2 atmosphere at a bias of −40 V.

As will be seen in this paper, measurements on these devices indicate that conduction in the ultrathin transistor involves one or at most two layers of pentacene, even at low gate fields. In ultrathin transistors, therefore, this process may be considered as essentially two-dimensional. Indeed, in the presence of a gate field larger than 0.5 MV cm^{-1}, the accumulated charges are fully confined to the first layer. We will also demonstrate further on that the ultrathin film transistors have no contact resistances and can therefore be used as a model system. As well, thanks to these properties, we will be able to validate a very simple two-dimensional transport picture, different from the classical FET models [17, 18], which illustrates the crucial role played by oxide surface defects in determining the transistor properties.

Figure 1 presents the measured current–voltage characteristics of our OFETs and illustrates the extreme sensitivity of OFET performance to film thickness. Indeed, a close look at this figure

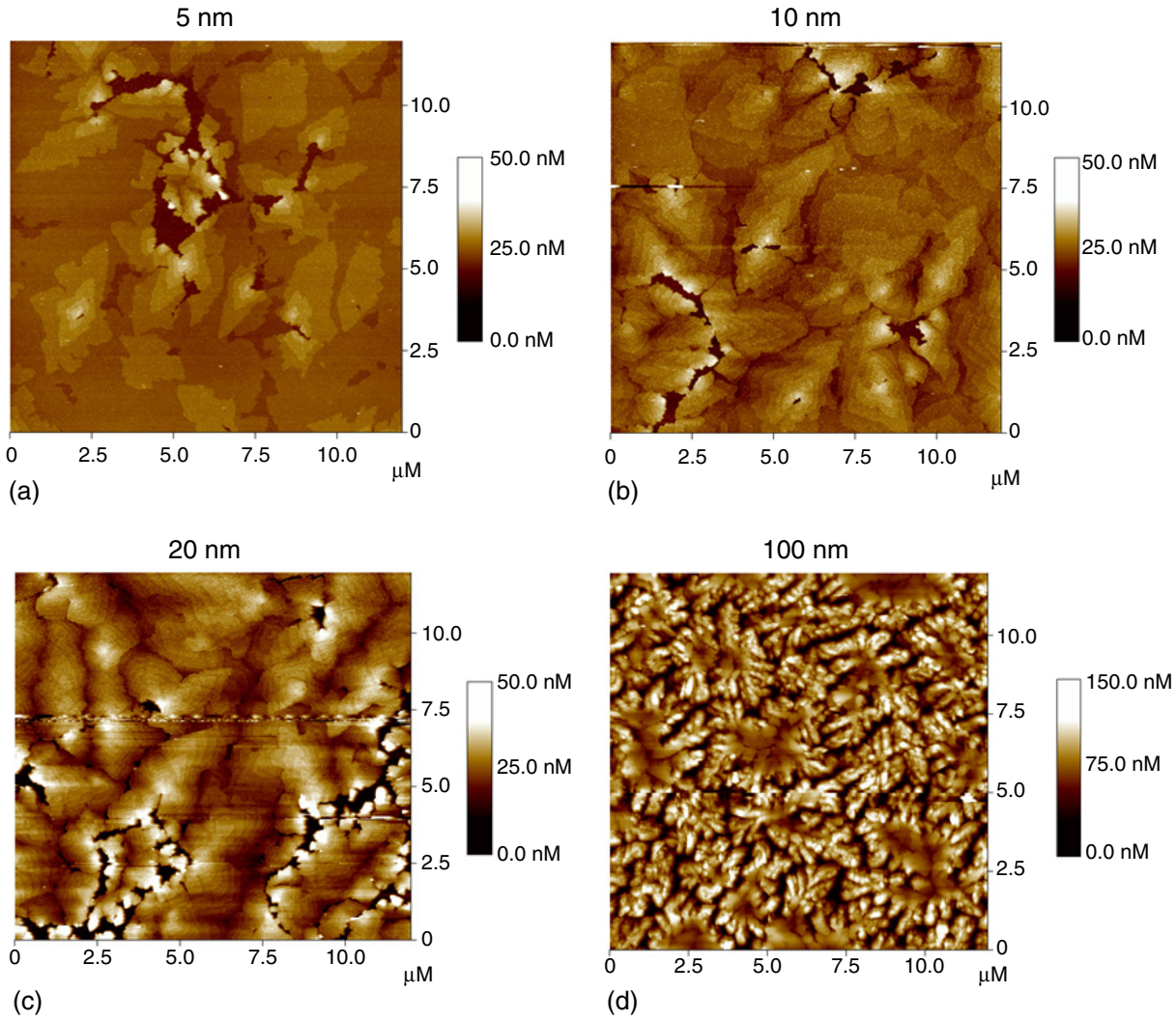

Figure 2. AFM images of the conduction channel. The channel morphology changes as the film thickness is increased. The best film structure is in the ultrathin transistor while the worst (dendritic) is in the 100 nm thick pentacene film where the bulk imperfections determine the film growth process.

shows that the drain current I_D has its maximal value for the ultrathin pentacene transistor and then, surprisingly, drops, in a rather drastic way, as the pentacene thickness increases. Thus, the thinner the pentacene film, the more efficient the transistor in figure 1.

Let us first discuss this phenomenon from the viewpoint of film growth morphology, which is, in fact, thickness dependent. In figure 2, the best pentacene morphology is seen to be in the ultrathin transistor where atomic force microscopy images demonstrate full coverage of the adjacent pentacene islands and minimal inter-island boundary density. In particular, to assist the formation of large pentacene grains in the first monolayers on the oxide surface, a substrate temperature and deposition rate of 338 K and 0.6 nm min^{-1}, respectively were maintained. Details of the growth conditions may be found in [9, 10]. These values are optimal for the construction of ultrathin pentacene film layers; however, for thicker films, the growth mechanism competes

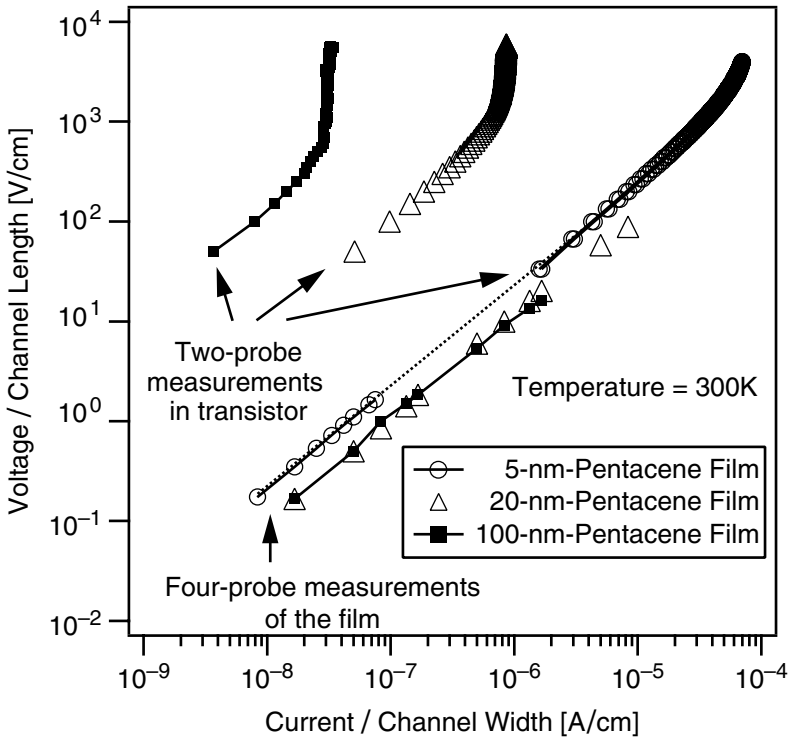

Figure 3. Four-probe and two-probe resistivity measurements of the pentacene film. In the 5 nm ultrathin film transistor, the two- and four-probe resistivities coincide indicating that the contact resistance is negligible. In the 20 and 100 nm thick pentacene film OFETs, however, the probes/organic contact resistance becomes a crucial factor for the electrical transport properties. This phenomenon is due to the difficulty of transport from the gold contacts, through the granular bulk, to the semiconducting layer.

with various coarsening (reconstruction) processes. Thus, inter-island grain boundaries or other crystalline singularities will tend to dominate the bulk of the film. The inset in figure 1 provides an artist's view of this granular morphology in thick films. Obviously, when the source–drain current flows across the top contacts, the bulk structural imperfections present large potential barriers to the propagation of charge [19].

In figure 1, the different electrical characteristics of OFETs at different thicknesses can also be analysed in terms of the contact resistances of the films. We have investigated two different film-contact geometries: the classical two-probe geometry in which the resistance of the contacts affects the measurements of the intrinsic resistance of the film and the four-probe geometry which eliminates the contact resistance [18]. The results presented in figure 3 show that the contact resistance is negligible in the ultrathin transistor, while at higher thicknesses it dominates the transistor current.

Our pentacene films can thus be considered as lamellar structures [20] where only one or two layers close to the oxide are enough to offer a conducting channel for the carriers. This fact is clearly established by the four-probe resistivity measurements on films thicker than 10 nm. Indeed, in figure 3 the 20 and 100 nm thick pentacene films exhibit the same two-dimensional

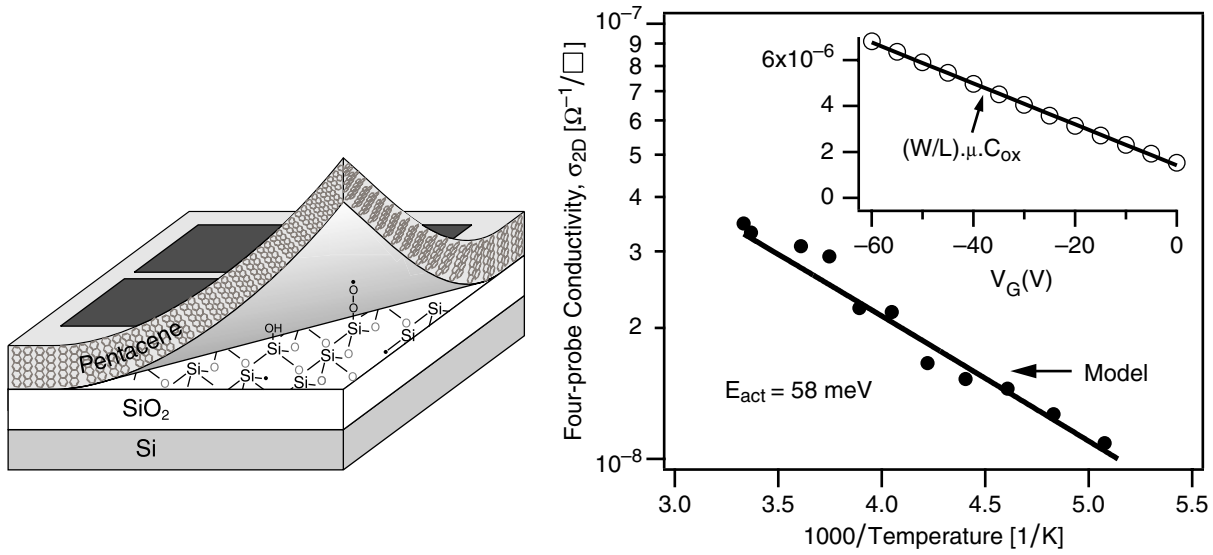

Figure 4. (A) Sketch of the pentacene/SiO_2 interface below the pentacene single layer; and (B) intrinsic film two-dimensional conductivity σ_{2D} as a function of temperature. The decline of σ_{2D} with T^{-1} is due to a decrease of the hole density p_{holes} in the first layer; Upper inset: the field-effect mobility μ of the ultrathin OFETs ($\sim 0.1\,cm^2\,V^{-1}\,s^{-1}$) is calculated from the slope of I_D/V_D versus V_G (transconductance), which itself was derived from the linear regime of the current-voltage transistor characteristics. Here the mobility is independent of the gate voltage due to the absence of contact resistance.

resistivity ρ_{2D} at $V_G = 0$. This is fundamentally different from the case of homogeneous films where this transport property should scale inversely with the film thickness. The intrinsic film resistivity ρ_{2D} is found, in fact, to be $35\,M\Omega\,\square^{-1}$ which we tend to attribute essentially to the first layer resistance, in agreement with the calculations presented below.

Indeed, when a gate voltage is applied to pentacene OFETs, one can show, in fact, that the above effect is even enhanced. Previous studies have demonstrated that the charge carrier mobility in OFETs reaches its highest value as the thickness approaches approximately two monolayers [21]. Thus, conduction in the ultrathin pentacene transistor can be interpreted in terms of a two-dimensional process.

This single active monolayer of pentacene obviously interacts strongly with the oxide surface. However, this interaction is not generally considered in an explicit way in most works concerning OFETs. In some, for example, a somewhat 'mysterious' threshold field is introduced at gate fields close to zero to include the main thermodynamic interface effects. Here we propose a different picture, where both the oxide surface and the active pentacene layer are treated as a whole. In this approach, the oxide is not just a homogenous passive dielectric but an active surface in the sense that electroactive surface defects and radicals (peroxy-radicals $\equiv$ Si–O–O$^{\bullet}$, E'-centres $\equiv$ Si$^{\bullet}$, non-bridging oxygen hole centres $\equiv$ Si–O$^{\bullet}$ [22]–[24]) can act as electron acceptors (or hole traps from a pentacene viewpoint). This is particularly true when the surface has been exposed to moisture or, as in our case, to a short, low-energy plasma discharge which activated it prior to the fabrication of the transistor (see figure 4(a)).

Although many possible defects/traps could be active on such a surface, we shall show that the present results can be interpreted quantitatively in terms of a single electron-acceptor trap. Different types of radicals have been recently identified on oxide (SiO_2, TiO_2, Al_2O_3) surfaces [23, 25]. One of them is particularly active on SiO_2: the peroxy-radicals [23, 24]. These oxygen-active defects can accept electrons from the pentacene molecules. Similar to electrochemical reactions in a polar-liquid phase, the charge-transfer reactions at the oxide–pentacene interface are made possible by the solid-state charge-solvation process. Both oxide and pentacene are polar so that their electronic levels are shifted significantly with respect to the single molecule case [26].

Experimental proof for the existence of these charge transfer reactions can be found in the four-probe measurements on pentacene films in figure 3. These measurements were also repeated systematically for many of the other samples. Obviously, Ohm's law observed over several current decades at zero gate field (see the slope in figure 3) indicates the presence of a few ppm of residual holes transferred from the oxide surface into the pentacene lattice. In this approach, very simple equations can be written to describe the interface equilibrium. The chemical potential ε_F of either electrons trapped on peroxy-radicals or holes transferred to the pentacene molecules can be expressed by the usual Langmuir isotherm on the oxide side [27] and narrow-band statistics on the pentacene side. Thus

$$\varepsilon_F = \Delta\varepsilon - k_B T \ln\left(\frac{R}{n} - 1\right), \tag{1}$$

where $\Delta\varepsilon = \varepsilon_- - E$ is the difference between the electron affinity of the radicals ε_- and ionization potential E of the pentacene molecules (solvation effects included), R is the radical density on SiO_2 per unit area, and n is the density of the electrons (cm^{-2}) trapped on the radical levels.

According to Fermi–Dirac statistics, the hole density p_{holes} (cm^{-2}) in pentacene is

$$p_{\text{holes}} = \int_{+4J}^{-4J} D(\varepsilon) f(\varepsilon, \varepsilon_F)\, \mathrm{d}\varepsilon = \frac{P k_B T}{4\,|J|} \ln\left[\frac{1 + \exp\left(-\frac{4J+\varepsilon_F}{k_B \cdot T}\right)}{1 + \exp\left(\frac{4J-\varepsilon_F}{k_B \cdot T}\right)}\right], \tag{2}$$

where $D(\varepsilon)$ is the two-dimensional density of states per unit area and unit energy, $f(\varepsilon, \varepsilon_F)$ is the Fermi factor of the holes, $J < 0$ is the transfer integral in pentacene, P is the density of pentacene molecules per unit area and ε_F is the Fermi level of the carriers defined with respect to the centre of the pentacene band with width $8|J|$.

At thermal equilibrium, the two-dimensional charge transfer on the pentacene molecules/SiO_2 interface is controlled by the equilibrium of the chemical potentials ε_F from equations (1) and (2). The residual carrier density at $V_G = 0$ satisfies the condition $p_{\text{holes}} = n$. Furthermore, when a negative V_G potential is applied to the SiO_2 gate dielectric, the carrier density in the first layer of OFETs will be the sum of the residual carrier density of the film and the field-effect charge density accumulated on the dielectric semiconductor interface:

$$p_{\text{holes}} = -\frac{C_{\text{ox}}\, V_G}{q} + n = \frac{C_{\text{ox}}}{q}(V_T - V_G), \quad q > 0,\ V_G < 0, \tag{3}$$

where C_{ox} is the electrical capacity of the gate oxide (19.5 nF cm^{-2}). The residual carrier concentration n determines the threshold field $V_T = (qn)/C_{\text{ox}}$ in the ultrathin transistor. Besides,

$n = p_{\text{holes}}$ also determines the two-dimensional conductivity from the four-probe measurements (see figure 4(b)):

$$\sigma_{2D} = p_{\text{holes}}\, q\, \mu, \tag{4}$$

where μ is the hole mobility.

From the transconductance characteristics (see upper inset in figure 4(b)) calculated from the linear regime of an ultrathin transistor, we deduce both the field effect mobility at room temperature $\mu = 0.1\,\text{cm}^2\,\text{V}^{-1}\,\text{s}^{-1}$ and the threshold voltage $V_{\text{T}} = +16\,\text{V}$. Note that the mobility is not gate-voltage dependent because of the absence of contact resistance. The intrinsic conductivity is found to be about 2.86×10^{-8} Siemens $\square$ (see equation (4)) so that the residual concentration of carriers is $n(300\,\text{K}) = p_{\text{holes}}\,(300\,\text{K}) = 1.88 \times 10^{12}\,\text{cm}^{-2}$. Furthermore, we have neglected the temperature variation of the mobility since this is in agreement with many recent reports [28, 29], and have attributed the measured conductivity activation energy (~58 meV) in figure 4(b) to the variation of trapped electron concentrations on the oxide surfaces. One can also estimate the position of the Fermi level at room temperature $\varepsilon_F = 345\,\text{meV}$ with respect to the centre of the pentacene band, the charge transfer integral $|J| = 75\,\text{meV}$, the charge transfer energy $\Delta\varepsilon = 400\,\text{meV}$ and the radical concentration $R = 5 \times 10^{12}\,\text{cm}^{-2}$.

Despite its extreme simplicity, the transistor model presented here, which is based on only one type of trap (peroxy radicals, for instance) on the dielectric surface shows the importance of describing the charge transfers at the interface. It is particularly successful in determining the pertinent transfer integral $|J|$ in pentacene, the value of which is consistent with the renormalization theory [26] and quantum chemistry calculations [20]. Moreover, the positive threshold field in the ultrathin transistor discussed in this paper can be entirely attributed to the residual carrier concentration through $V_T = (nq)/C_{\text{ox}}$. Although there is good agreement between the model and transistor data, the above relation cannot be generalized, as a negative threshold voltage may also be obtained in some transistors measured in the literature [8, 16]. In fact, in addition to hosting high concentrations of potential traps, the oxide surfaces are also particularly dipolar. Large dipoles can influence the threshold gate field of transistors built on this dielectric surface depending on the relative compositions (cations and anions) of the first oxide layers. Consequently, we believe that the oxide monopolar and dipolar effects add, in general, their strength to determine the threshold field. In our pentacene transistor, for instance, the plasma treatments on the oxide surface have essentially favoured monopoles.

The present model based on a single trap site is far from being general. But here it works in the sense that it explains quantitatively two types of independent transport measurements as functions of temperature and fields.

In conclusion, the ultrathin OFETs in this paper have successfully been used as model systems for describing the charge carrier propagation in pentacene layers and transport phenomena on the pentacene/oxide interface. The carrier transport is dominated by the first semiconducting layer where the plasma activated electron traps on the oxide interface induce equal amounts of residual holes, which determine the transistor transport characteristics and performance. Consequently, the oxide and pentacene layers should be treated together as a two-dimensional system. Finally, this work has stimulated us to reach the limit in ultrathin transistor fabrication and to understand the charge-transport processes at the interface between the pentacene and the SiO_2 gate dielectric so fundamental to applications.

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